SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

FIELD

The present disclosure relates to a semiconductor device and in particular, to a semiconductor device with a better electrical performance and a method of manufacturing a semiconductor device.

BACKGROUND

A significant trend throughout integrated circuit (IC) development is the downsizing of IC components. As the size reduces, the performance requirements become more stringent. Also, as devices continue to shrink in size, the channel region continues to shrink as well. For metal-oxide-semiconductor field effect transistors (MOSFETs), increased performance requirements have generally been met by aggressively scaling the length of the channel region. However, such a short channel length faces high electric field and manufacturing limits.

As the length of a channel continues to shrink, diffusion of dopants becomes much harder to control. There are various thermal processes throughout a semiconductor manufacturing. For example, after dopants are implanted into a substrate, a thermal process is used to activate the dopants. However, these thermal processes cause dopant diffusion in an unintentional way. In addition, shorter channel lengths suffer from fluctuation of higher implantation concentration and depth. As the dopant concentration reaches about 1E20 atoms/cm^3, the dopants will easily diffuse into channel regions and induce short channel effects during a thermal process. The electrical properties, such as threshold voltage, are altered and deviated from a predetermined value. This causes uniformity between each device and is a severe problem in circuit design. As such, a sufficient method to control the doped profile is required.

BRIEF DESCRIPTION OF THE DRAWINGS

Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

FIG. **1** is a semiconductor device in accordance with some embodiments of the present disclosure.

FIG. **2** is a semiconductor device in accordance with some embodiments of the present disclosure.

FIGS. **3A-3E** are cross-sectional diagrams illustrating a manufacturing process of the semiconductor device of FIG. **2** in accordance with some embodiments of the present disclosure.

DETAILED DESCRIPTION

The following disclosure provides many different embodiments, or examples, for implementing different features of the provided subject matter. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

Further, spatially relative terms, such as "beneath," "below," "lower," "above," "upper" and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

The terms "wafer" and "substrate," as used herein, are to be understood as including silicon, silicon-on-insulator (SOI) technology, silicon-on-sapphire (SOS) technology, doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor foundation, and other semiconductor structures. Furthermore, when reference is made to a "wafer" or "substrate" in the following description, previous processing steps may have been utilized to form regions, junctions, or material layers in or over the base semiconductor structure or foundation. In addition, the semiconductor need not be silicon-based, but could be based on silicon-germanium, germanium, gallium arsenide or other semiconductor structures.

The terms "deposition" and "deposit," as used herein, refer to operations of depositing materials on a substrate using a vapor phase of a material to be deposited, a precursor of the material, and an electrochemical reaction or sputtering/reactive sputtering. Depositions using a vapor phase of a material include any operations such as, but not limited to, chemical vapor deposition (CVD) and physical vapor deposition (PVD). Examples of vapor deposition methods include hot filament CVD, rf-CVD, laser CVD (LCVD), conformal diamond coating operations, metal-organic CVD (MOCVD), thermal evaporation PVD, ionized metal PVD (IMPVD), electron beam PVD (EBPVD), reactive PVD, atomic layer deposition (ALD), plasma enhanced CVD (PECVD), high density plasma CVD (HDPCVD), low pressure CVD (LPCVD), and the like. Examples of deposition using an electrochemical reaction include electroplating, electro-less plating, and the like. Other examples of deposition include pulse laser deposition (PLD) and atomic layer deposition (ALD).

As the length of a channel region continues to shrink in a semiconductor device, diffusion of dopants becomes much harder to control. There are various thermal processes throughout a semiconductor manufacturing. However, these thermal processes cause dopant diffusion in an unintentional way. Diffused dopants may penetrate into a channel region. A gate barrier (band structure) is implemented for induced lowering by the diffused dopants in the channel region. As such, the unintentional dopants cause drain induced barrier lowering (DIBL) degradation. Drain induced barrier lowering (DIBL) is a short-channel effect in metal oxide semiconductor field-effect transistors (MOSFETs), referring to a reduction of threshold voltage of the transistor at higher drain voltages. In a MOSFET with a long channel, the bottleneck in the channel formation occurs far enough from